REMARKS

Applicants have amended claim 1. Claims 17-25 are withdrawn from consideration. Claims 1-16 are pending.

In the Office Action, the Examiner rejected claims 1-13 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Mattson et al. (U.S. Patent No. 6,4266,991) in view of Chappo et al. (U.S. Patent No. 6,510,195); and rejected claim 16 under 35 U.S.C. § 103(a) as being unpatentable over Mattson et al. in view of Chappo et al. and Yamanaka (U.S. Patent No. 6,372,558). Applicants traverse these objections, at least for the following reasons.

The Examiner has not applied any rejection to claim 14. Accordingly, Applicants submit that claim 14 should now be in condition for allowance.

Applicants traverse the rejections applied to remaining claims 1-13, 15, and 16 at least because the applied references do not disclose or suggest any of Applicants' claimed combinations wherein the thickness of each recessed portion is thinner than the thickness of a portion around the recessed portion. In connection with this point, it is useful to refer to Applicants' specification for background discussion relating to, but not limiting of, such claimed subject matter.

As a first point, in the paragraph beginning at page 4, line 4, Applicants' specification states that:

"Since the back illuminated photodiode array of the invention is provided with the second conductive type semiconductor regions at the bottom of the recessed portions formed on an opposite surface, it is possible to make a distance between the light-incident surface of the semiconductor substrates and the semiconductor regions shorter, thereby it is possible to inhibit a phenomenon that a carrier generated by incident light that undergoes recombination during a transferring process, then a higher detection sensitivity is kept on. Furthermore, the recessed portions can be formed in an array." (Underlining added.)

Then, in the paragraph beginning at page 5, line 11, Applicants' specification states that:

"More particularly, a distance between the light-incident surface and the second conductive type semiconductor region, i.e., the surface where photodiodes are arranged is determined by the thickness of the first semiconductor substrate. Since the first semiconductor substrate can be made thinner by the existence of the frame part surrounded by the recessed portions, while it keeps the mechanical strength carrier generated inside the semiconductor substrate will move at a shorter distance. Thus, the recombination of carriers are inhibited to maintain a higher detection sensitivity of the back illuminated photodiode array." (Underlining added.)

Thus, a plurality of recessed portions may be utilized to reduce the distance between the light-incident surface of the semiconductor substrates and the semiconductor regions, which in turn makes it possible to inhibit carrier recombination so as to maintain a higher detection sensitivity. And, at the same time, a frame structure surrounding the recessed portions can be configured so that the frame portion around each recessed portion is thicker than the thickness of recessed portion which it surrounds, which provides mechanical strength. In other words, the thinness of the recessed portions allows higher detection sensitivity while at the same time the thickness of the frame portion provides mechanical strength. Thus, a structure combining the two may be high in both detection sensitivity and mechanical strength.

In contrast to the subject matter recited in Applicants' independent claim 1, the applied Mattson et al. referenced purportedly discloses a back illuminated photodiode (BIP) array comprising a first conductive type flat semiconductor substrate having a light-incident surface (Fig. 3). However, Applicants submit that this substrate does not have a plurality of recessed portions as recited Applicants' claim 1.

Applicants submit that Chappo et al. does not make up for the deficiencies of Mattson et al. While the Examiner appears to be alleging that Chappo et al. discloses a plurality of recessed portions in its Figures 2 to 4, Applicants submit that there is no disclosure in this reference of

any recessed portions such as recited in Applicants' claim 1. In this regard, reference number 52 in Chappo et al. is said to correspond to a BIP array, reference numeral "54" is said to refer to contact pads, reference numeral "10" is said to correspond to a CT scanner, and reference numeral "120" is said to refer to a peripheral side surface. In other words, Chappo et al. is said to disclose a back illuminated photodiode (BIP) array 52 comprising a first conductive type semiconductor substrate having a light-incident surface (Fig. 2A), but Applicants submit that the substrate is flat and therefore does not have a plurality of recessed portions as recited in Applicants' independent claim 1. More particularly, the Mattson et al. and Chappo et al. references do not disclose or suggest Applicants' claimed combinations wherein the thickness of each recessed portion is thinner than the thickness of a portion around the recessed portion, nor does the applied Yamanaka et al. reference make up for this deficiency.

At this time, Applicants now point out what appear to be misunderstandings on the Examiner's part about certain aspects of the present application. It is hoped that the presentation of the following remarks will help clarify the Examiner's understanding as to each of these points and the operation and construction of the invention overall.

In this regard, the Examiner states, at page 8, line 10, of the Office Action, that "Applicants' first contention that Mattson elements 42/64 are daughter board." Applicants assume that the Examiner intended to refer to "142" rather than "42" in this statement. Moreover, reference element "64" appears to designate a daughter board and reference element "142" appears to designate ceramic substrate.

Moreover, the Examiner refers at page 9, lines 8 to 13, of the Office Action, to "a plurality of recessed portions next to bond pads 54 on B-I-P array 52 and located opposite said

light incident surface (substrate 58). * * * Therefore even assuming arguendo Applicants' argument is correct, still Chappo teaches/describes an opposite surface with a plurality of recessed portions located opposite said light incident surface." However, Applicants submit that neither Mattson et al. nor Chappo et al. shows or suggests any recessed portions (e.g., depressions or concaves). In this regard, Applicants ask that the Examiner please note that a pn junction is formed at the bottom of each of the recessed portions recited in Applicants' independent claim 1.

The Examiner also states, at page 9, lines 1 to 3, of the Office Action, that "which when further gleaned from figure 7 clearly shows substrates 42/64 to be substrate having a light-incident surface, it is further noted that by definition semiconductors are conducting. However, Applicants assume that the Examiner intended to refer to "142" rather than "42" in this sequence and point out that reference numeral "64" is believed to be designating a daughter board. One definition of the term daughter board, (from Daughter Board - "http://www.computerhope.com/jargon/d/daughter.htm"), states that: "Also known as piggyback boards, daughter boards are expansion boards that commonly connect directly to the motherboard and give the computer an added feature such as modem capability. Today, these types of boards are not found or used in desktop computers and have been replaced with ISA or PCI boards. However, many laptops use these types of boards." In view of the foregoing, Applicants submit that Mattson et al. merely discloses a BIP array (50) or (140) arranged on a daughter board (64) or ceramic substrate (142) as shown in Fig. 7 or Fig. 12 of that reference.

The Examiner goes on to state, at page 9, lines 4 to 6, in the Office Action, that "Applicants' next contention that Chappo in figure 10, #120 and col. 11 lines 4-8 does not

describe an opposite surface with a plurality of recessed portions located opposite said light-incident surface . . ." However, this position also fails in view of the actual language of Chappo et al. In particular, col. 11, lines 4-8, of Chappo states that: "metal layers can be placed in notches or recesses formed in a peripheral edge 120 so as to prevent electrical contact between the metal layers 122 and adjacent readout ASICs when tiled together to form a mosaic." Nonetheless, this reference to recesses in Chappo et al. relates to the recesses formed at peripheral edge 120 (see Fig. 10, col. 11, line 5, for example) which do not correspond to the recesses defined in Applicants' independent claim 1.

The Examiner then states, at page 10, lines 8 to 10, of the Office Action, that "Chappo additionally in figure 2, 4 describes BIP 52 and recessed portions next to bumps 54 as shown above." Nevertheless, Applicants cannot locate any relevant recess portions within the teachings of the applied references, specifically, any recessed portion having a pn junction associated therewith and corresponding to those recited in Applicants' independent claim 1.

For at least the foregoing reasons, Applicants submit that independent claim 1, and each of the dependent claims depending therefrom, patentably distinguish over the references applied to the claims in the pending Office Action. Accordingly, reconsideration and withdrawal of all rejections set fort in the pending Office Action are respectfully requested.

CONCLUSION

In view of the foregoing, Applicants submit that the pending claims are in condition for allowance, and respectfully request reconsideration and timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of this

response, the Examiner is invited to contact Applicants' undersigned representative to expedite prosecution. A favorable action is awaited.

EXCEPT for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 50-0573. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

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